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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/747,806 | 12/29/2003 | Ajay K. Sinha | P17380 | 1851 |

28062 7590 09/15/2008

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| EXAMINER | |
|---|---|
| ZHOU, YONG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2619 | |
| **MAIL DATE** | **DELIVERY MODE** |
| 09/15/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/747,806 | SINHA ET AL. | |
| | Examiner | Art Unit | |
| | Yong Zhou | 2619 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11, 13-18, 20-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, Hyung Won et al. (US 2004/0049613), referred to hereinafter as Kim, in view of Nogle, Scott George et al. (US 5,781,480), referred to hereinafter as Nogle.

**Regarding claim 1**, Kim teaches a method (process, Abstract, line 1) comprising:

providing a link memory to store linked pointers for controlling access to a packet memory (Fig. 4, #400-402, [0025], lines 2-3 and 8-9, wherein the Free Pointer memory is provided to store free pointer queues (or free pointer linked lists) for controlling packet memory);

maintaining at least two free link lists in the link memory, each free link list indicating a respective linked set of free storage locations in the packet memory, said at least two free link lists including a first free link list and a second free link list (p3, left col., lines 2-5, [0028], lines 4-7, wherein the Balanced Linked List can have more than two Free Pointer queues to store independent free pointer linked lists).

However, Kim does not specifically teach that two memory allocation requests are serviced in one clock cycle.

Nogle teaches that a control circuit controls access to the memory cells, where substantially simultaneous requests for access are serviced sequentially within a single cycle of a clock signal of a data processor that is accessing the memory (Abstract, lines 5-9, col. 2, lines 61 through col. 3, line 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine teachings from Nogle into the Kim invention to serve two memory allocation requests in one clock cycle to achieve predictable results.

**Regarding claim 7**, Kim teaches an apparatus comprising:

a link memory to store linked pointers for controlling access to a packet memory (Fig. 4, #400-402, [0025], lines 2-3 and 8-9, wherein the Free Pointer memory is provided to store free pointer queues (or free pointer linked lists) for controlling packet memory); and

a memory controller (Fig. 2b, #230, [0009], lines 7-8) coupled to the link memory and operative to:

maintain at least two free link lists in the link memory, each free link list indicating a respective linked set of free storage locations in the packet memory, said at least two free link lists including a first free link list and a second free link list (p3, left col., lines 2-5, [0028], lines 4-7, wherein the Balanced Linked List can

have more than two Free Pointer queues to store independent free pointer linked lists).

However, Kim does not specifically teach that two memory allocation requests are serviced in one clock cycle.

Nogle teaches that a control circuit controls access to the memory cells, where substantially simultaneous requests for access are serviced sequentially within a single cycle of a clock signal of a data processor that is accessing the memory (Abstract, lines 5-9, col. 2, lines 61 through col. 3, line 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine teachings from Nogle into the Kim invention to serve two memory allocation requests in one clock cycle to achieve predictable results.

**Regarding claim 14**, Kim teaches a system comprising:

a packet memory (Fig. 4, #440-449) to store packet data;

a link memory to store linked pointers for controlling access to the packet memory (Fig. 4, #400-402, [0025], lines 2-3 and 8-9, wherein the Free Pointer memory is provided to store free pointer queues (or free pointer linked lists) for controlling packet memory); and

a memory controller (Fig. 2b, #230, [0009], lines 7-8) coupled to the link memory and operative to:

maintain at least two free link lists in the link memory, each free link list indicating a respective linked set of free storage locations in the packet memory,

said at least two free link lists including a first free link list and a second free link list (p3, left col., lines 2-5, [0028], lines 4-7, wherein the Balanced Linked List can have more than two Free Pointer queues to store independent free pointer linked lists).

However, Kim does not specifically teach that two memory allocation requests are serviced in one clock cycle.

Nogle teaches that a control circuit controls access to the memory cells, where substantially simultaneous requests for access are serviced sequentially within a single cycle of a clock signal of a data processor that is accessing the memory (Abstract, lines 5-9, col. 2, lines 61 through col. 3, line 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine teachings from Nogle into the Kim invention to serve two memory allocation requests in one clock cycle to achieve predictable results.

**Regarding claim 21**, Kim teaches an apparatus comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

maintaining at least two free link lists in the link memory, each free link list indicating a respective linked set of free storage locations in the packet memory, said at least two free link lists including a first free link list and a second free link list (p3, left col., lines 2-5, [0028], lines 4-7, wherein the Balanced Linked List can

have more than two Free Pointer queues to store independent free pointer linked lists).

However, Kim does not specifically teach that two memory allocation requests are serviced in one clock cycle.

Nogle teaches that a control circuit controls access to the memory cells, where substantially simultaneous requests for access are serviced sequentially within a single cycle of a clock signal of a data processor that is accessing the memory (Abstract, lines 5-9, col. 2, lines 61 through col. 3, line 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine teachings from Nogle into the Kim invention to serve two memory allocation requests in one clock cycle to achieve predictable results.

**Regarding claims 2 and 22**, Kim further teaches that each of the free link lists is permitted to point to any storage location in the packet memory, except that no link in any of the free link lists points to a free link in another free link list ([0026], lines 1-5, wherein the two free pointer queues are disjoined and the free pointers in all free pointer queues can cover entire memory).

**Regarding claims 3 and 23**, Kim further teaches that each of the free link lists includes a plurality of pointers, each pointer indicating a corresponding storage location in the packet memory and a corresponding storage location in the link memory (Fig. 4, #400-402, [0035], line 5 through p4, left col., line 8, wherein the free pointer in each of

the free pointer queues points to the corresponding storage location in the packet memory; the pointer also indicates the storage location in the free pointer queues #401, #402).

**Regarding claims 4 and 24**, Kim further teaches:

in each clock cycle in which a memory allocation request is serviced, allocating storage locations from the packet memory that are pointed to by a one of the free link lists ([0028], lines 2-4, [0030], lines 2-3, wherein the retrieving the free pointer to store one new element of packet data can be performed every clock cycle) that is, at the time of said each clock cycle, at least as large as any other of the free link lists ([0026], lines 5-8, wherein all the free pointer queues are maintained balanced in length).

**Regarding claims 5 and 25**, Kim further teaches:

in each clock cycle in which storage locations in the packet memory are freed, assigning a freed linked set of pointers in the link memory to a one of the free link lists ([0029], lines 1-6, [0030], lines 1-3, wherein the returning the free pointer to the free pointer queue when an element of packet data is freed can be performed every clock cycle) that is, at the time of said each clock cycle, at least as small as any other of the free link lists ([0026], lines 5-8, wherein all the free pointer queues are maintained balanced in length).

**Regarding claims 6 and 26**, Kim further teaches that more than two free link lists are maintained in the link memory (p3, left col., lines 2-5, [0028], lines 4-7, wherein the Balanced Linked List can have more than two Free Pointer queues to store independent free pointer linked lists).

**Regarding claims 8-11 and 13**, Kim teaches the limitations of claim 7. They contain the same limitations as claims 2-6, respectively. Therefore, they are rejected for the same reasons.

**Regarding claims 15-18 and 20**, Kim teaches the limitations of claim 14. They contain the same limitations as claims 2-6, respectively. Therefore, they are rejected for the same reasons.

3. Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Nogle and Najam, Zahid et al. (US 2002/194291), referred to hereinafter as Najam.

**Regarding claims 12 and 19**, Kim and Nogle teach the limitations of claims 7 and 14, respectively.

Kim and Nogle do not specifically teaches that the link memory is a dual port memory.

Najam teaches that the dual port memory is used to place pointers ([0118], lines 2-3.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine teachings from Najam into the Kim and Nogle invention to include the dual port memory for the link memory.

### *Response to Arguments*

4. Applicant's arguments, filed July 14, 2008, have been considered but are moot in view of the new ground(s) of rejection.

See more details above.

### *Conclusion*

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yong Zhou whose telephone number is (571)270-3451. The examiner can normally be reached on Monday - Friday 8:00am - 5:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag G. Shah can be reached on (571) 272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yong Zhou

September 2, 2008

/Chirag G Shah/
Supervisory Patent Examiner, Art Unit 2619